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10/802,914	03/18/2004	Kazutoshi Funahashi	2004_0425A	5409

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EXAMINER	
GOLDEN, JAMES R	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/802,914	FUNAHASHI ET AL.	
	Examiner	Art Unit	
	James Golden	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11 May 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The instant application 10/802914 has a total of 19 claims pending. There are 3 independent claims and 16 dependent claims.

Information Disclosure Statement

1. The information disclosure statement submitted on 05/11/2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file. Priority has been granted to the Japanese application filed on 03/19/2003.

Specification

3. The abstract is objected to because of the following informalities: the presence of the drawing elements 10, 20 and 21. This objection may be overcome by removing the elements from the abstract.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1, 3, 5-11 and 19** are rejected under 35 U.S.C. 102(e) as being anticipated by Farmer et al. (US 6,725,369), filed April 28, 2000.

6. **With respect to claim 1**, Farmer et al. disclose a processor **(220 of Fig. 2; column 2, lines 47-48)** connected to a memory **(240 of Fig. 2; column 3, lines 39-40)** via a data bus **(system data bus 280 and processor data bus 250 of Fig. 1; column 2, lines 56-58)**, comprising

- an address conversion unit **(software on processors 210 and 220 of Fig. 2)** operable to
  - convert at least one lower bit of an address so as to indicate a reversed position of data in the data bus **(column 3, lines 33-34)**, and
  - output the converted address to the memory **(column 3, lines 31-33)**, when the second processor performs a memory access for the data with a smaller width than the data bus **(Fig. 1 and column 1, lines 13-15 describe how a word is eight bytes long; column 2, line 66 -- column 3, line 2 describe how the data buses may be varying widths)**,
- wherein the processor is connected to the data bus in a way that data is transmitted to and from the memory in a byte order based on an

endianness which is opposite to an endianness of said processor **(column 3, lines 40-43)**.

7. **With respect to claim 3**, Farmer et al. disclose the processor according to claim 1 (see above paragraph 6), executing a program that defines structure data which includes data that is smaller than a basic word length **(Fig. 1; column 1, lines 11-18, where words are composed of bytes)**, said structure data being shared between the processor and another processor of a different endianness **(210 of Fig. 2; column 2, line 47)** via the memory **(processors 210 and 220 connected through memory 240; column 2, lines 56-59)**, said data being defined in an order within the basic word length **(column 1, lines 11-18)**, and said order being in reverse to an order in a definition of said structure data in a program to be executed by said another processor **(column 2, lines 48-52)**.

8. **With respect to claim 5**, Farmer et al. disclose a data sharing apparatus comprising a first processor **(210 of Fig. 2; column 2, lines 47)**, a second processor **(220 of Fig. 2; column 2, line 47-48)**, and a memory **(240 of Fig. 2; column 3, lines 39-40)**, said first and second processors being of different endianness **(column 2, lines 48-52)**, wherein both the first processor and the second processor are connected to the memory via a data bus **(system data bus 280 of Fig. 1; column 2, lines 56-58)**, in a byte order based on the endianness of the first processor **(processor 210 and memory 240 of Fig. 2 are both big endian)**.

9. **With respect to claim 6**, Farmer et al. disclose the data sharing apparatus according to claim 5 (see above paragraph 8), further comprising an

address conversion unit **(software on processors 210 and 220 of Fig. 2)** operable to

- convert at least one lower bit of an address so as to indicate a reversed position of data in the data bus **(column 3, lines 33-34)**, and
- output the converted address to the memory **(column 3, lines 31-33)**, when the second processor performs a memory access for the data with a smaller width than the data bus **(Fig. 1 and column 1, lines 13-15 describe how a word is eight bytes long; column 2, line 66 -- column 3, line 2 describe how the data buses may be varying widths)**.

10. **With respect to claim 7**, Farmer et al. disclose the data sharing apparatus according to claim 6 (see above paragraph 9), further comprising a transfer unit **(interface 230 of Figs. 2 and 3; column 2, lines 56-57; column 3, lines 19-22, lines 26-29)** operable to control data transfer by direct memory access **(column 3, lines 21-22 and lines 29-30)**, wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the data bus is to be transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination **(column 3, lines 6-7, lines 19-22 and lines 26-30)**.

11. **With respect to claim 8**, Farmer et al. disclose the data sharing apparatus according to claim 7 (see above paragraph □), wherein the transfer unit includes a conversion unit **(software on processors 210 and 220 of Fig. 2)** operable to convert at least one lower bit of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus

(column 3, lines 33-34), and output the converted address to the memory **(column 3, lines 31-33)**, in the case where a source and a destination require data of different endianness **(column 3, lines 40-43)** and data with a smaller width than the data bus is to be transferred **(Fig. 1 and column 1, lines 13-15 describe how a word is eight bytes long; column 2, line 66 -- column 3, line 2 describe how the data buses may be varying widths)**.

12. **With respect to claim 9**, Farmer et al. disclose the data sharing apparatus according to claim 6 (see above paragraph 9),

- wherein the memory stores structure data to be accessed by a first processor and a second processor **(column 3, lines 39-40)**,
- the first processor executes a first program that defines the structure data **(column 2, lines 48-50)**, and
- the second processor executes a second program that defines structure data **(column 2, lines 50-52)** which includes data that is smaller than the basic word length, said data being defined in an order within the basic word length **(Fig. 1; column 1, lines 11-18, where words are composed of bytes)**, and said order being in reverse to an order in the first program **(column 2, lines 48-52)**.

13. **With respect to claim 10**, Farmer et al. disclose the data sharing apparatus according to claim 9 (see above paragraph 12), further comprising a transfer unit **(interface 230 of Figs. 2 and 3; column 2, lines 56-57; column 3, lines 19-22, lines 26-29)** operable to control data transfer by direct memory access **(column 3, lines 21-22 and lines 29-30)**, wherein, in the case where a

source and a destination require data of different endianness and data with a smaller width than the data bus is to be transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination **(column 3, lines 6-7, lines 19-22 and lines 26-30)**.

14. **With respect to claim 11**, Farmer et al. disclose the data sharing apparatus according to claim 10 (see above paragraph 13), wherein the transfer unit includes a conversion unit **(software on processors 210 and 220 of Fig. 2)** operable to convert at least one lower bit of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus **(column 3, lines 33-34)**, and output the converted address to the memory **(column 3, lines 31-33)**, in the case where a source and a destination require data of different endianness **(column 3, lines 40-43)** and data with a smaller width than the data bus is to be transferred **(Fig. 1 and column 1, lines 13-15 describe how a word is eight bytes long; column 2, line 66 -- column 3, line 2 describe how the data buses may be varying widths)**.

15. **With respect to claim 19**, Farmer et al. disclose a method of sharing data in a data processing apparatus which includes a first processor **(210 of Fig. 2; column 2, lines 47)** and a second processor **(220 of Fig. 2; column 2, lines 47-48)** of different endianness **(column 2, lines 48-52)**, and a memory **(240 of Fig. 2; column 3, lines 39-40)** to which both the first processor and the second processor are connected via a data bus **(system data bus 280 of Fig. 1; column 2, lines 56-58)**, in a byte order based on the endianness of the first

processor **(processor 210 and memory 240 of Fig. 2 are both big endian)**, the method comprising:

- a step of causing the second processor to execute a program that defines structure data **(column 2, lines 50-52)** which includes data that is smaller than a basic word length **(Fig. 1; column 1, lines 11-18, where words are composed of bytes)**, said structure data being shared in the memory **(column 3, lines 39-44)**, said data being defined in an order within the basic word length **(column 1, lines 11-18)**, and said order being in reverse to an order in a definition of said structure data for the first processor **(column 2, lines 48-52)**, and
- a conversion step of converting at least one lower bit of an address so as to indicate a reversed position of data in the data bus **(column 3, lines 33-34)**, in the case where the second processor performs a memory access for data with a smaller width than the data bus **(Fig. 1 and column 1, lines 13-15 describe how a word is eight bytes long; column 2, line 66 -- column 3, line 2 describe how the data buses may be varying widths)**.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which

said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. **Claims 2, 4 and 12-18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Farmer et al. (US 6,725,369), filed April 28, 2000, in view of Heeb et al. (US 5,74,923), published November 12, 1996.

18. **With respect to claim 2**, Farmer et al. disclose the processor according to claim 1 (see above paragraph 6). Farmer et al. do not disclose the limitations further comprising a cache memory connected to the data bus in a byte order based on the endianness of the processor, wherein the processor reads data from the memory through the cache memory in data units of the same width as the data bus.

However, Heeb et al. disclose the limitations further comprising a cache memory **(cache 16 of Fig. 1; column 3, line 49)** connected to the data bus **(MMB 14 of Fig. 1; column 3, line 50)** in a byte order based on the endianness of the processor **(column 4, lines 28-31)**, wherein the processor reads data from the memory through the cache memory in data units of the same width as the data bus **(column 5, lines 5-6)**.

Farmer et al. and Heeb et al. are analogous art because they are from the same field of endeavor, namely endian conversion.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the cache memory of Heeb et al. with the endian conversion system of Farmer et al. The motivation for doing so would have been because the cache "stores copies of data... for subsequent use by the

processor core" (column 4, lines 8-11) which allows the processor to operate faster.

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Heeb et al. with Farmer et al. for the benefit of an endian conversion system with a cache memory to obtain the invention as specified in claim 2.

19. **With respect to claim 4**, Farmer et al. disclose the processor according to claim 3 (see above paragraph 7), Farmer et al. do not disclose the limitations further comprising a cache memory connected to the data bus in a byte order based on the endianness of the processor, wherein the processor reads data from the memory through the cache memory in data units of the same width as the data bus.

However, Heeb et al. disclose the limitations further comprising a cache memory **(cache 16 of Fig. 1; column 3, line 49)** connected to the data bus **(MMB 14 of Fig. 1; column 3, line 50)** in a byte order based on the endianness of the processor **(column 4, lines 28-31)**, wherein the processor reads data from the memory through the cache memory in data units of the same width as the data bus **(column 5, lines 5-6)**.

20. **With respect to claim 12**, Farmer et al. disclose the processor according to claim 5 (see above paragraph 8). Farmer et al. do not disclose the limitations further comprising a cache memory connected to the data bus in a byte order based on the endianness of the second processor.

However, Heeb et al. disclose the limitations further comprising a cache memory **(cache 16 of Fig. 1; column 3, line 49)** connected to the data bus **(MMB 14 of Fig. 1; column 3, line 50)** in a byte order based on the endianness of the second processor **(column 4, lines 28-31)**.

21. **With respect to claim 13**, Farmer et al. disclose the processor according to claim 12 (see above paragraph 20), further comprising an address conversion unit **(software on processors 210 and 220 of Fig. 2)** operable to

- convert at least one lower bit of an address so as to indicate a reversed position of data in the data bus **(column 3, lines 33-34)**, and
- output the converted address to the memory **(column 3, lines 31-33)**, when the second processor performs a memory access for the data with a smaller width than the data bus **(Fig. 1 and column 1, lines 13-15 describe how a word is eight bytes long; column 2, line 66 -- column 3, line 2 describe how the data buses may be varying widths)**.

22. **With respect to claim 14**, Farmer et al. disclose the data sharing apparatus according to claim 13 (see above paragraph 21), further comprising a transfer unit **(interface 230 of Figs. 2 and 3; column 2, lines 56-57; column 3, lines 19-22, lines 26-29)** operable to control data transfer by direct memory access **(column 3, lines 21-22 and lines 29-30)**, wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the data bus is to be transferred, the transfer unit reverses an

order of said data within a basic word length, for the source and the destination **(column 3, lines 6-7, lines 19-22 and lines 26-30)**.

23. **With respect to claim 15**, Farmer et al. disclose the data sharing apparatus according to claim 14 (see above paragraph 22), wherein the transfer unit includes a conversion unit **(software on processors 210 and 220 of Fig. 2)** operable to convert at least one lower bit of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus **(column 3, lines 33-34)**, and output the converted address to the memory **(column 3, lines 31-33)**, in the case where a source and a destination require data of different endianness **(column 3, lines 40-43)** and data with a smaller width than the data bus is to be transferred **(Fig. 1 and column 1, lines 13-15 describe how a word is eight bytes long; column 2, line 66 -- column 3, line 2 describe how the data buses may be varying widths)**.

24. **With respect to claim 16**, Farmer et al. disclose the data sharing apparatus according to claim 13 (see above paragraph 21),

- wherein the memory stores structure data to be accessed by a first processor and a second processor **(column 3, lines 39-40)**,
- the first processor executes a first program that defines the structure data **(column 2, lines 48-50)**, and
- the second processor executes a second program that defines structure data **(column 2, lines 50-52)** which includes data that is smaller than the basic word length, said data being defined in an order within the basic word length **(Fig. 1; column 1, lines 11-18, where words are composed**

of bytes), and said order being in reverse to an order in the first program **(column 2, lines 48-52)**.

25. **With respect to claim 17**, Farmer et al. disclose the data sharing apparatus according to claim 16 (see above paragraph 24), further comprising a transfer unit **(interface 230 of Figs. 2 and 3; column 2, lines 56-57; column 3, lines 19-22, lines 26-29)** operable to control data transfer by direct memory access **(column 3, lines 21-22 and lines 29-30)**, wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the data bus is to be transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination **(column 3, lines 6-7, lines 19-22 and lines 26-30)**.

26. **With respect to claim 18**, Farmer et al. disclose the data sharing apparatus according to claim 17 (see above paragraph 25), wherein the transfer unit includes a conversion unit **(software on processors 210 and 220 of Fig. 2)** operable to convert at least one lower bit of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus **(column 3, lines 33-34)**, and output the converted address to the memory **(column 3, lines 31-33)**, in the case where a source and a destination require data of different endianness **(column 3, lines 40-43)** and data with a smaller width than the data bus is to be transferred **(Fig. 1 and column 1, lines 13-15 describe how a word is eight bytes long; column 2, line 66 -- column 3, line 2 describe how the data buses may be varying widths)**.

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Moyer (US 5,907,865) teaches a processor that can read little- and big-endian data from a memory.
- Carnevale et al. (US 5,687,337; EP 0729093) teach a single-endian processor with a bi-endian memory and a cache.
- Loen et al. (US 5,928,349; EP 0729094) also teach a single-endian processor with a bi-endian memory and a cache.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James R. Golden whose telephone number is 571-272-5628. The examiner can normally be reached on Monday-Friday, 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James R. Golden
Patent Examiner
Art Unit 2187

September 13, 2006

DONALD SPARKS
SUPERVISORY PATENT EXAMINER